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FIG. 1A

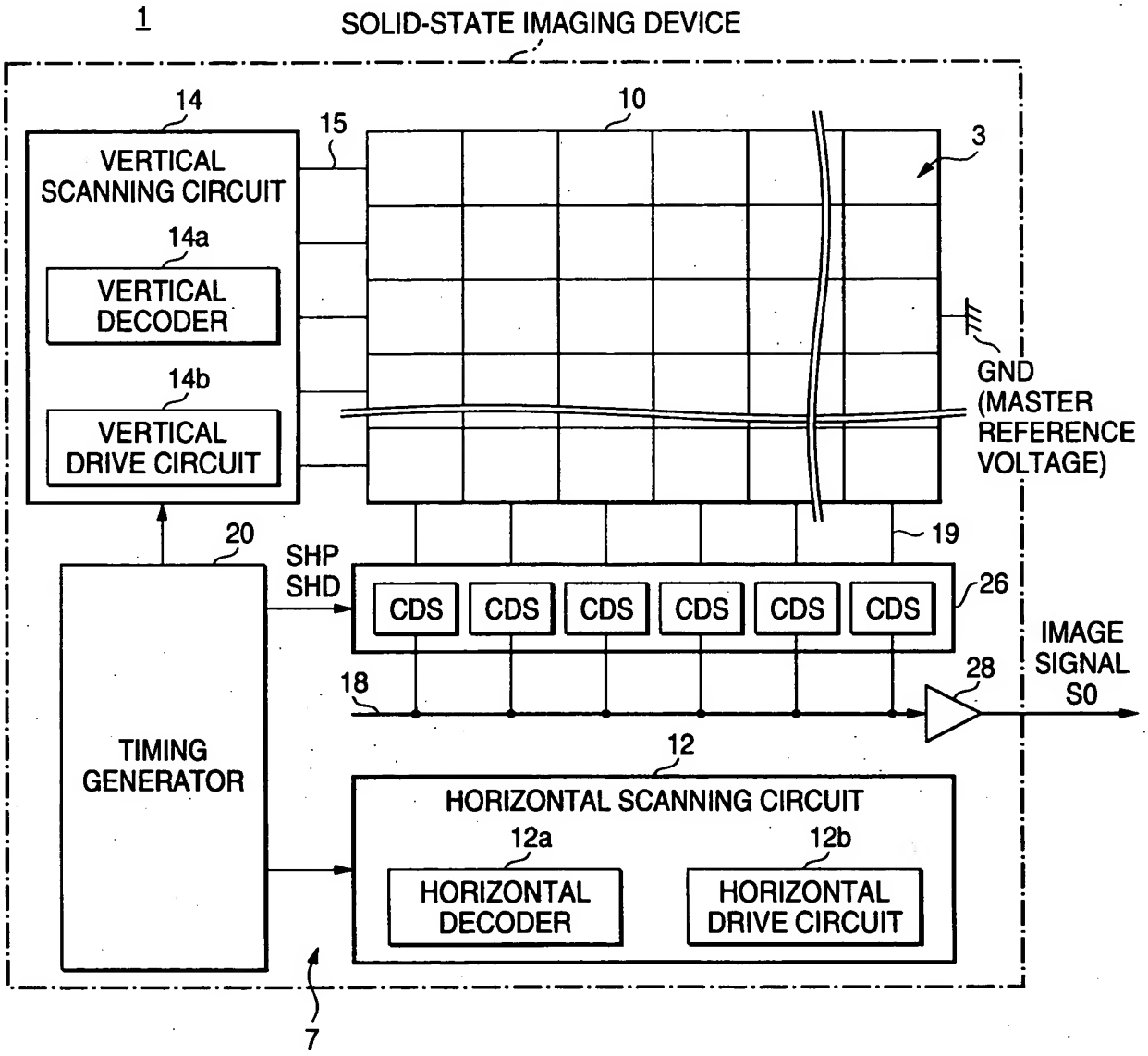
1
SOLID-STATE IMAGING DEVICE
14
VERTICAL SCANNING CIRCUIT
14a
VERTICAL DECODER
14b
VERTICAL DRIVE CIRCUIT
15
10
3
GND (MASTER REFERENCE VOLTAGE)
19
20
SHP
SHD
CDS
CDS
CDS
CDS
CDS
CDS
26
IMAGE SIGNAL S0
28
18
TIMING GENERATOR
12
HORIZONTAL SCANNING CIRCUIT
12a
HORIZONTAL DECODER
12b
HORIZONTAL DRIVE CIRCUIT
7

FIG. 1B

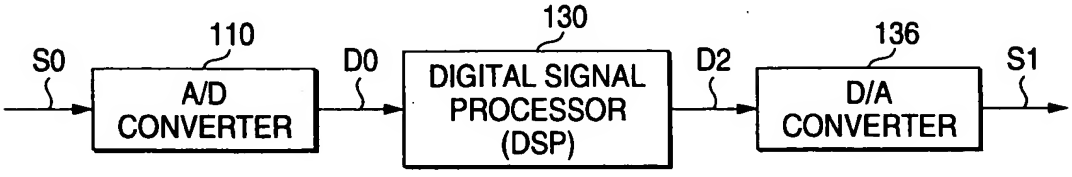
S0
110
A/D CONVERTER
D0
130
DIGITAL SIGNAL PROCESSOR (DSP)
D2
136
D/A CONVERTER
S1

FIG. 2A

*DEVICE STRUCTURE
- VGA-COMPATIBLE CMOS SENSOR (APPROX. 0.3 MILLION PIXELS)
- CLOCK FREQUENCY: 6MHz (FRAME RATE 13.3fps)
- UNIT PIXEL IN 3-TRANSISTOR STRUCTURE
- PIXEL PITCH 4.1μm

*DRIVE CONDITION
- POWER VOLTAGE 3.0V
- TRANSFER GATE DRIVE VOLTAGE HAVING VARIABLE LOW LEVEL
- OTHER DRIVING TO THE PIXEL BY 0V AND POWER VOLTAGE (3.0V)

FIG. 2B

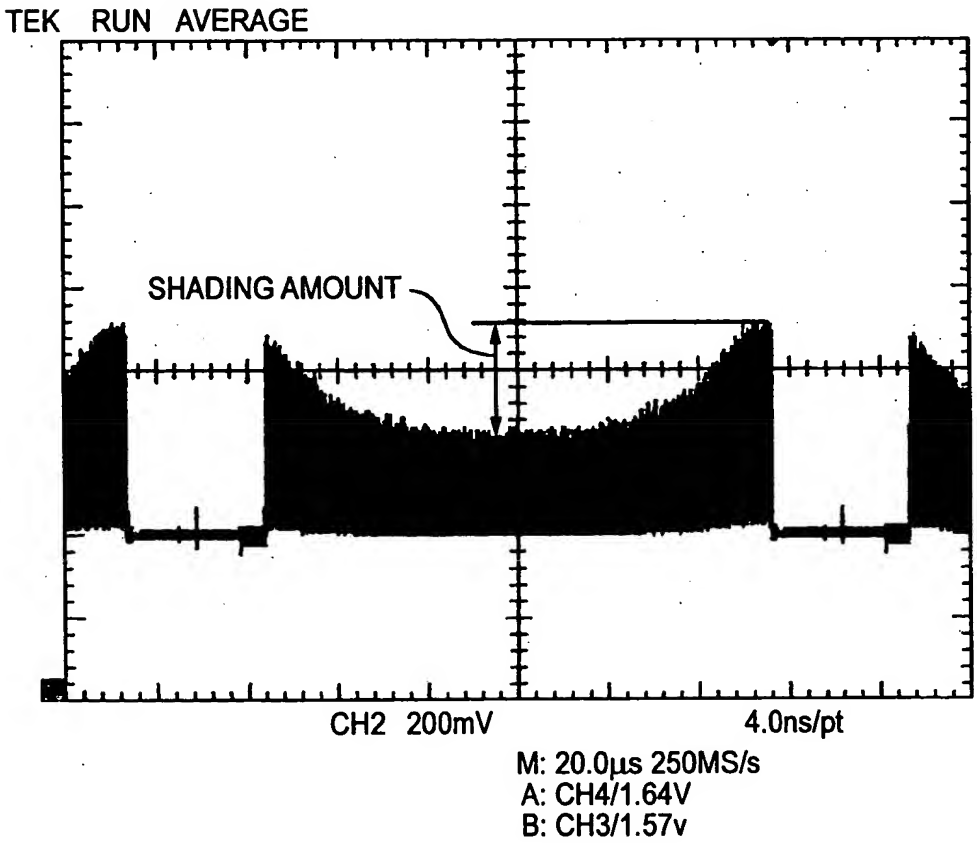

FIG. 3

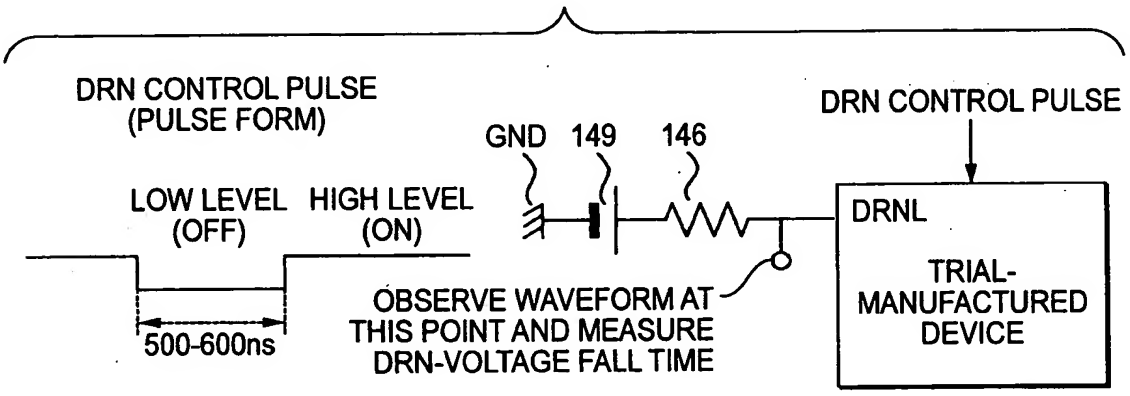
DRN CONTROL PULSE
(PULSE FORM)
LOW LEVEL
(OFF)
HIGH LEVEL
(ON)
500-600ns
GND
149
146
OBSERVE WAVEFORM AT
THIS POINT AND MEASURE
DRN-VOLTAGE FALL TIME
DRN CONTROL PULSE
DRNL
TRIAL-
MANUFACTURED
DEVICE

FIG. 4A

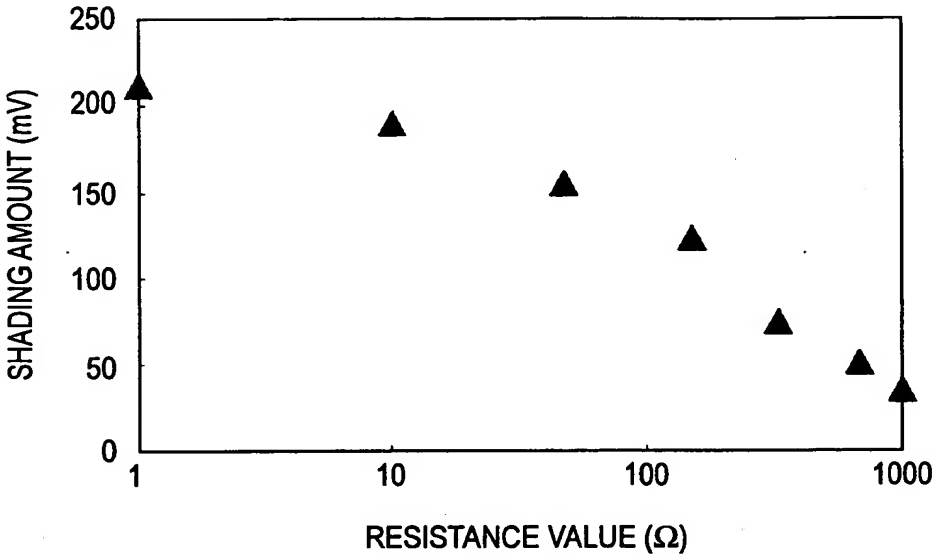
250
200
150
100
50
0
SHADING AMOUNT (mV)
1
10
100
1000
RESISTANCE VALUE (Ω)

FIG. 4B

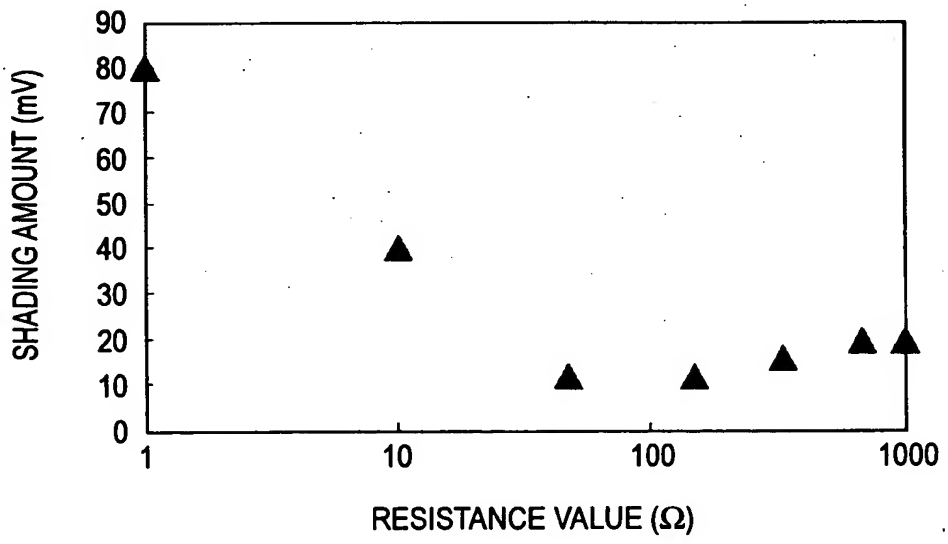
90
80
70
60
50
40
30
20
10
0
SHADING AMOUNT (mV)
1
10
100
1000
RESISTANCE VALUE (Ω)

FIG. 5A

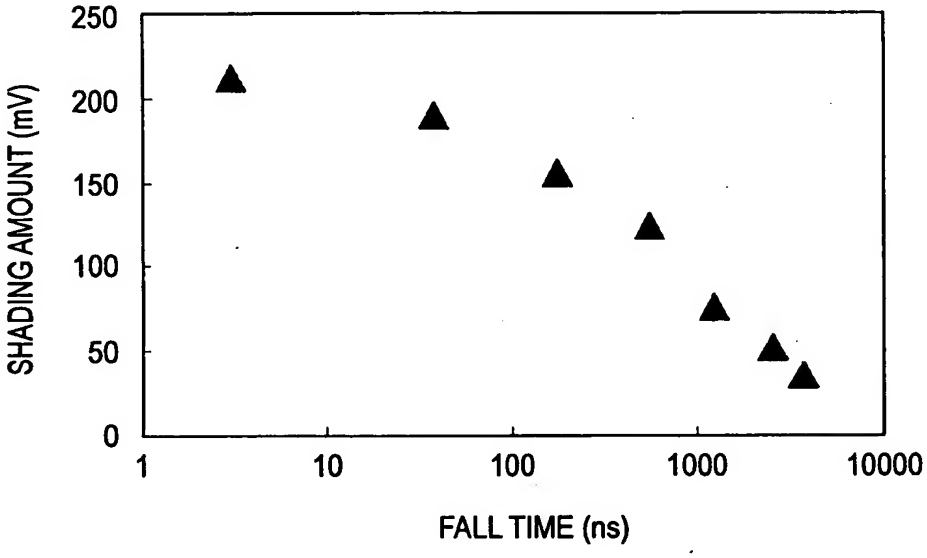
250
200
150
100
50
0
SHADING AMOUNT (mV)
1
10
100
1000
10000
FALL TIME (ns)

FIG. 5B

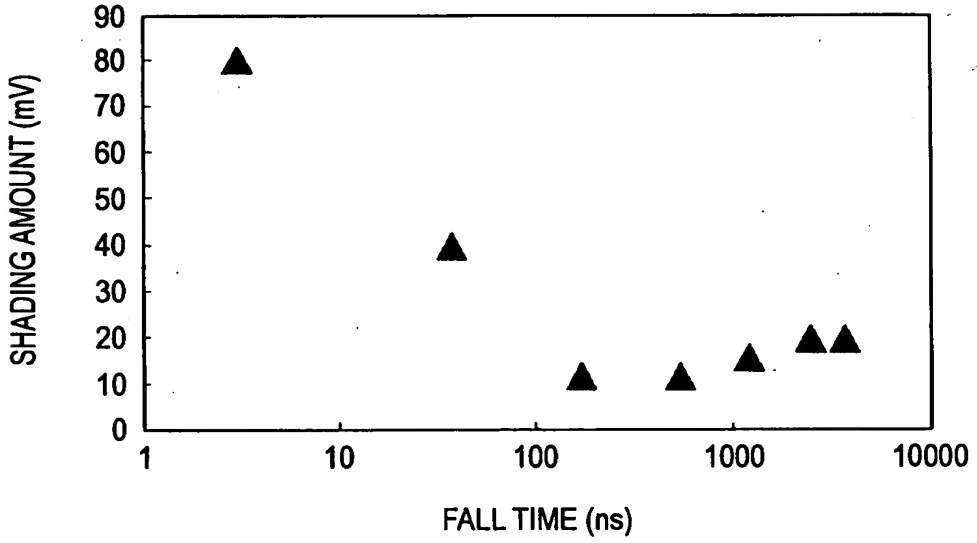
90
80
70
60
50
40
30
20
10
0
SHADING AMOUNT (mV)
1
10
100
1000
10000
FALL TIME (ns)

FIG. 6

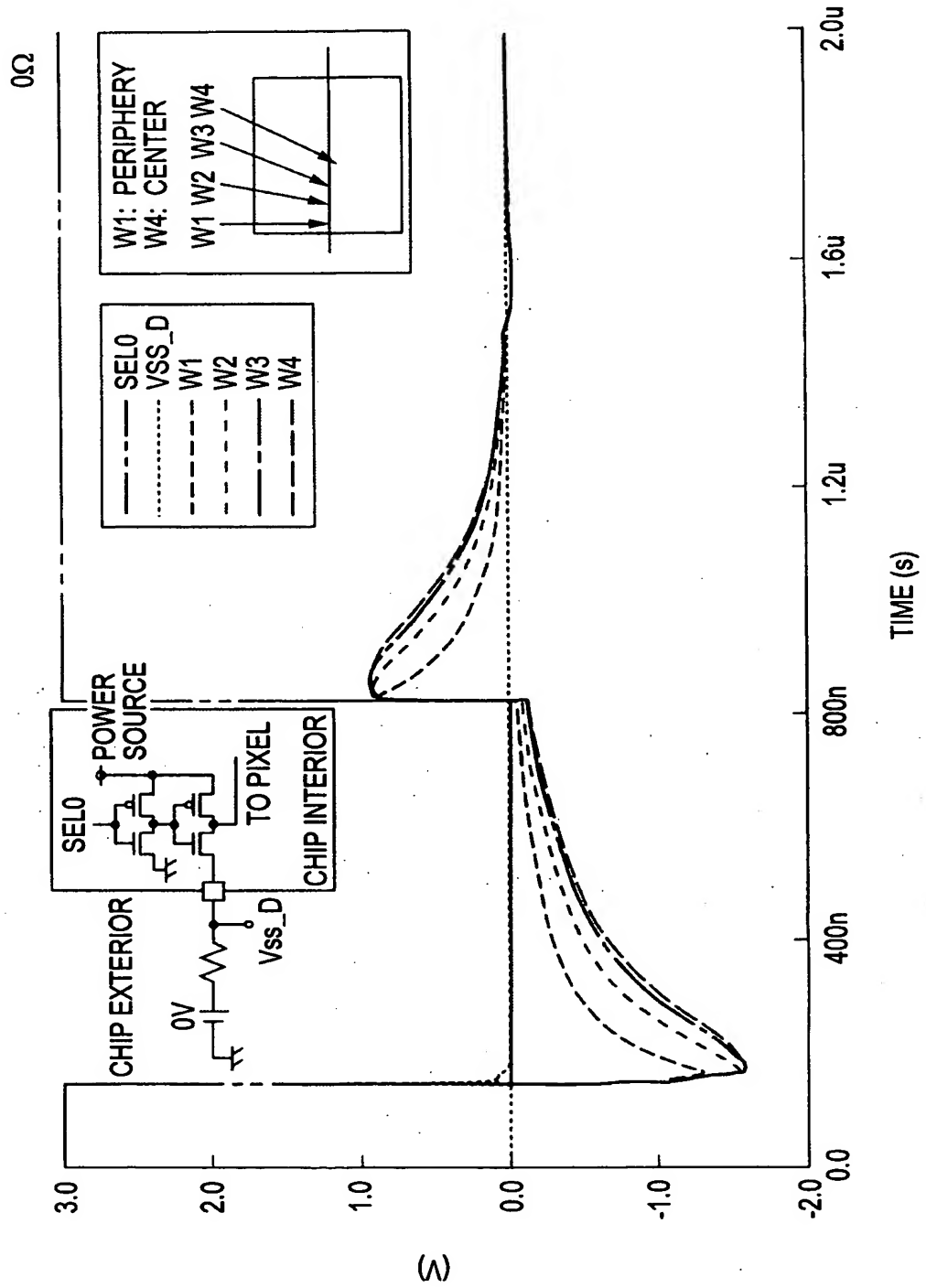
0Ω
W1: PERIPHERY
W4: CENTER
W1 W2 W3 W4
SEL0
VSS_D
W1
W2
W3
W4
POWER SOURCE
SEL0
TO PIXEL
CHIP INTERIOR
CHIP EXTERIOR
0V
Vss_D
3.0
2.0
1.0
0.0
-1.0
-2.0
(V)
0.0
400n
800n
1.2u
1.6u
2.0u
TIME (s)

FIG. 7

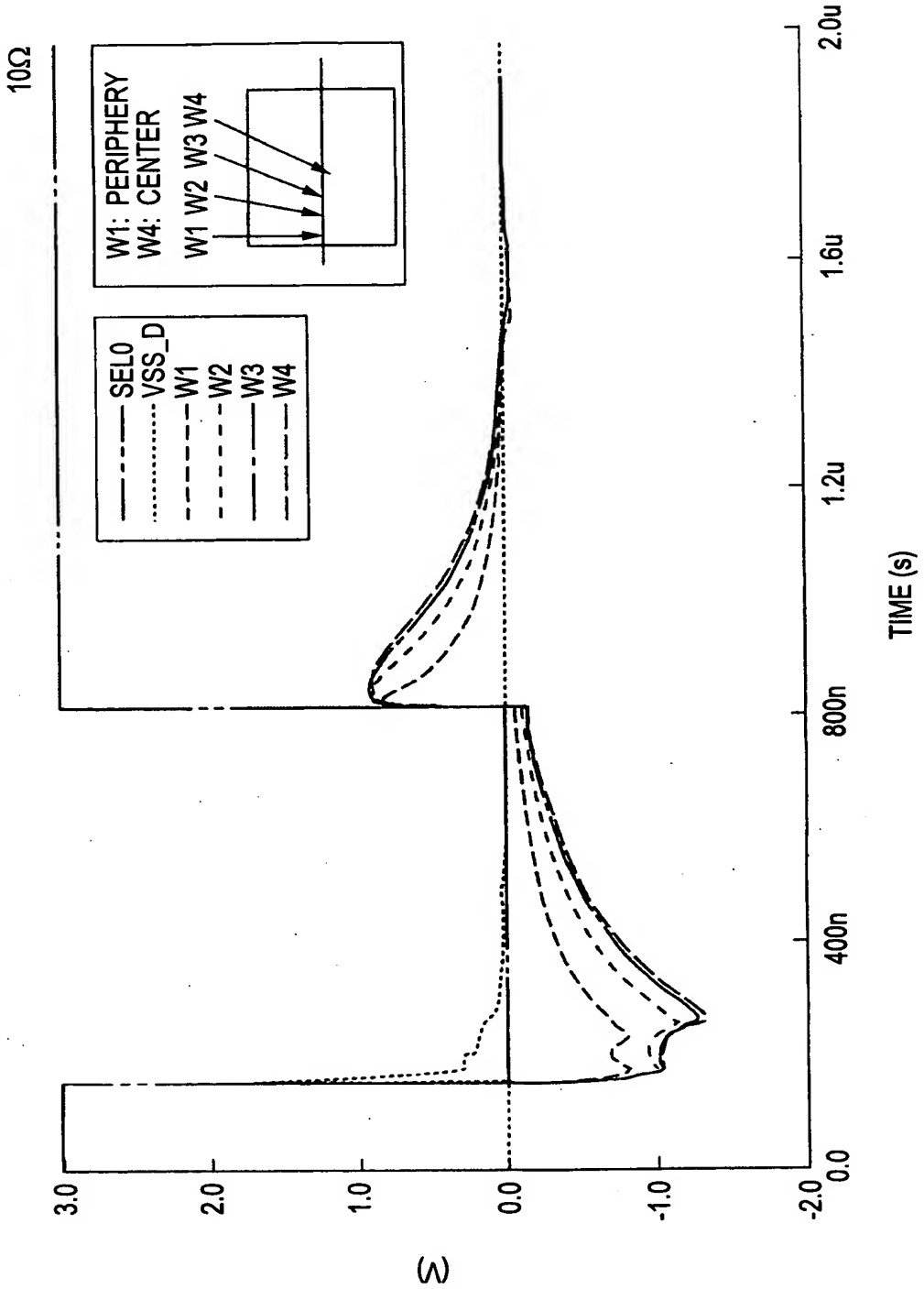
10Ω
W1: PERIPHERY
W4: CENTER
W1 W2 W3 W4
SEL0
VSS_D
W1
W2
W3
W4
3.0
2.0
1.0
0.0
-1.0
-2.0
(V)
0.0
400n
800n
1.2u
1.6u
2.0u
TIME (s)

FIG. 8

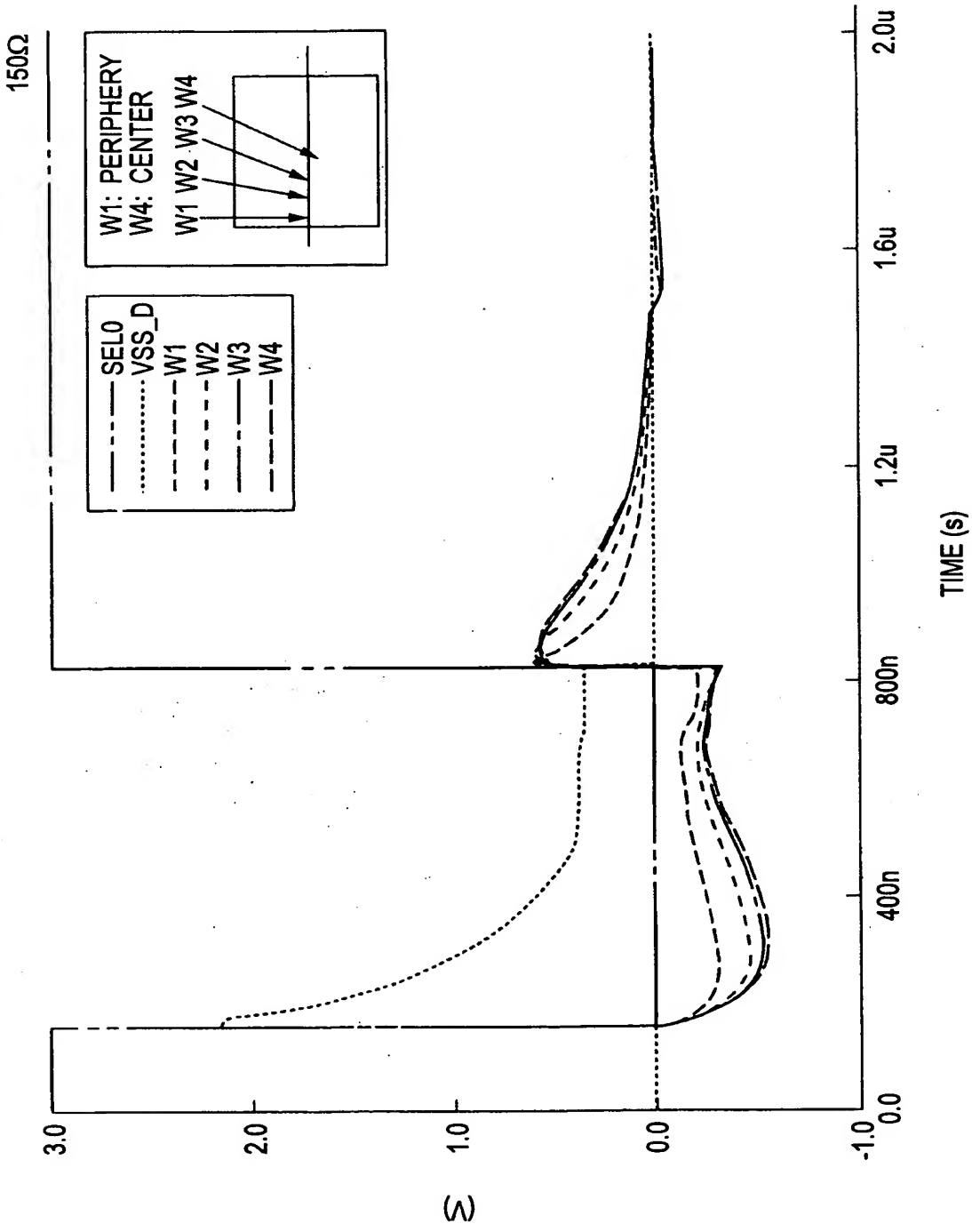
150Ω
W1: PERIPHERY
W4: CENTER
W1 W2 W3 W4
SEL0
VSS_D
W1
W2
W3
W4
3.0
2.0
1.0
0.0
-1.0
(V)
0.0
400n
800n
1.2u
1.6u
2.0u
TIME (s)

FIG. 9

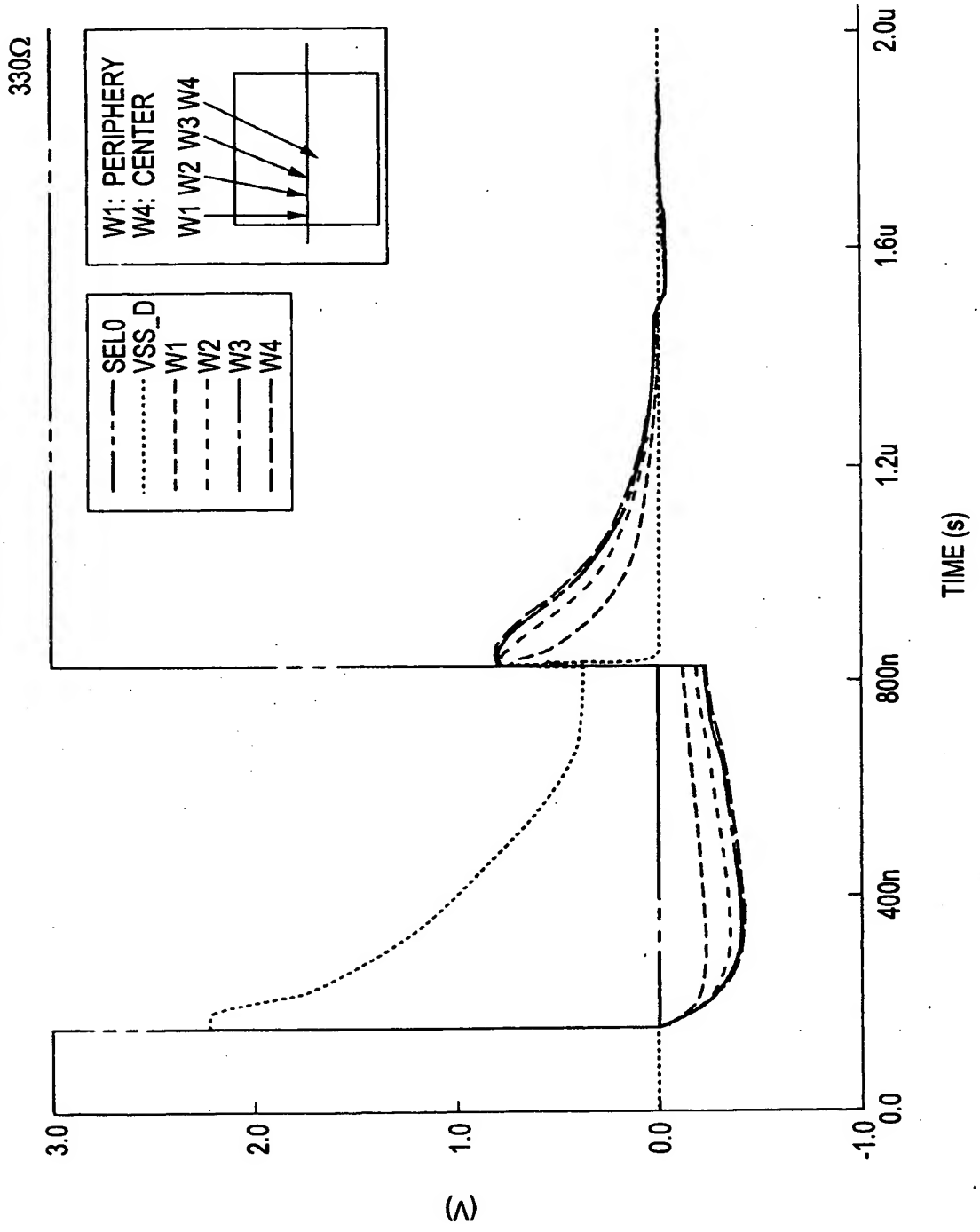
330Ω
W1: PERIPHERY
W4: CENTER
W1 W2 W3 W4
SEL0
VSS_D
W1
W2
W3
W4
3.0
2.0
1.0
0.0
-1.0
(V)
0.0
400n
800n
1.2u
1.6u
2.0u
TIME (s)

FIG. 10

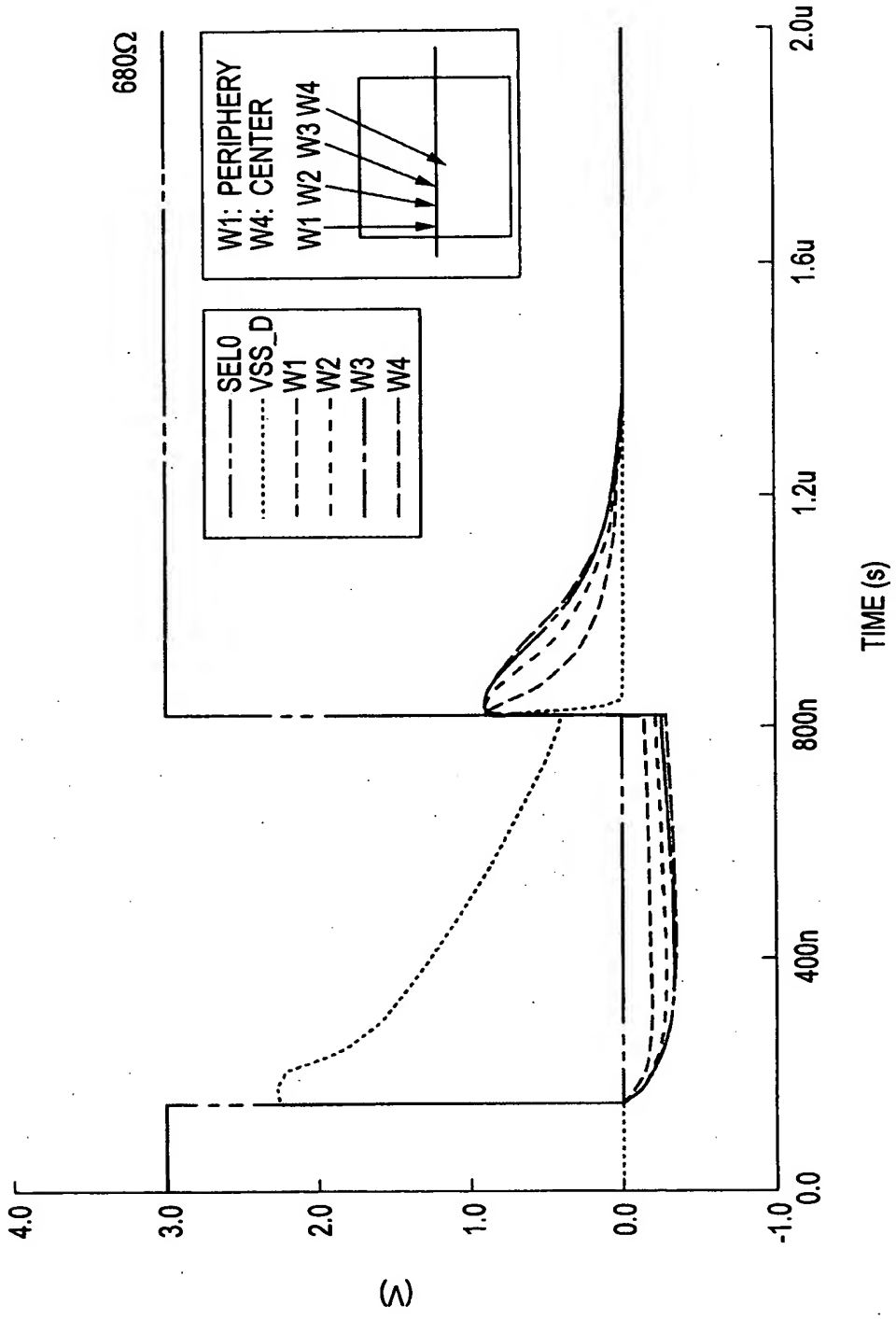
680Ω
W1: PERIPHERY
W4: CENTER
W1 W2 W3 W4
SEL0
VSS_D
W1
W2
W3
W4
4.0
3.0
2.0
1.0
0.0
-1.0
(V)
0.0
400n
800n
1.2u
1.6u
2.0u
TIME (s)

FIG. 11A

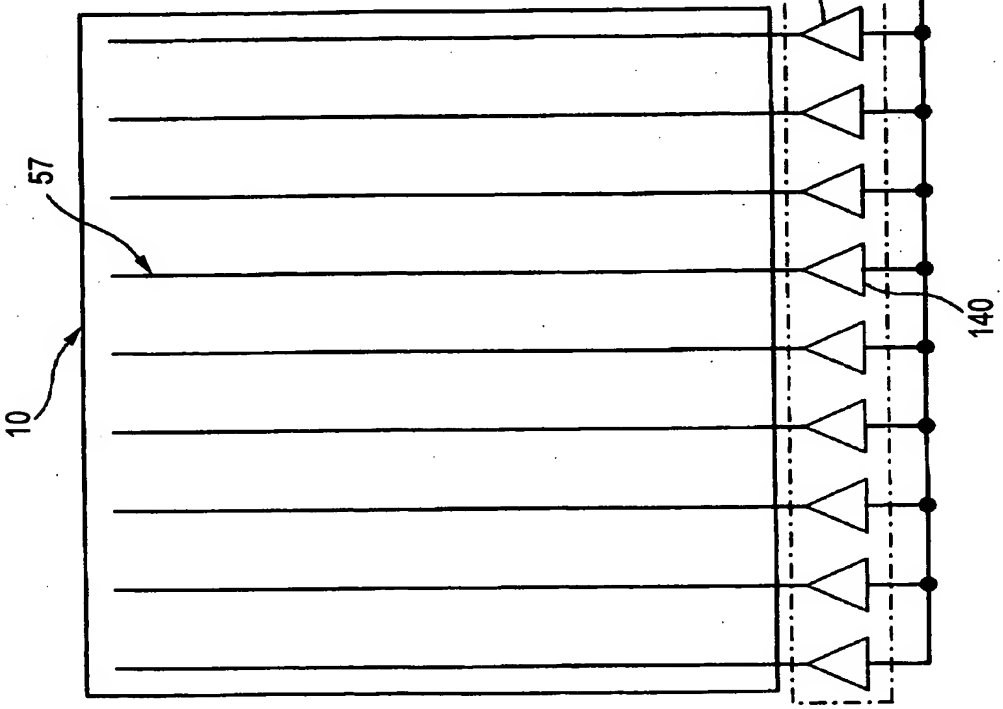

FIG. 11B

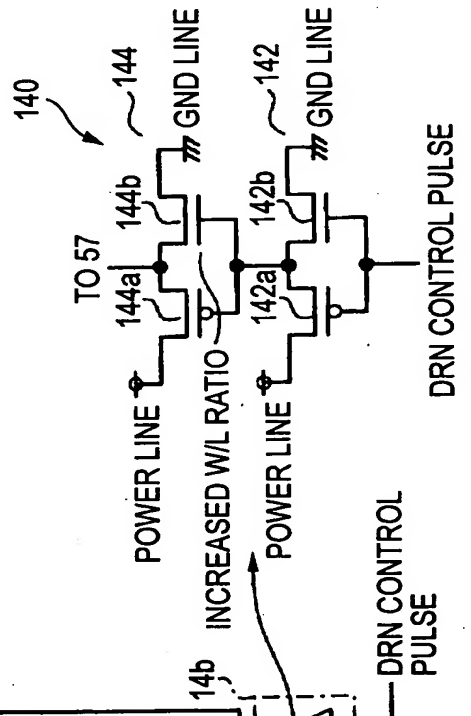

FIG. 11C

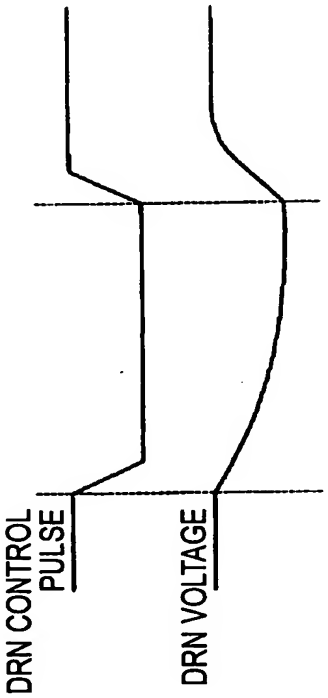

FIG. 12C

EXAMPLE OF BUFFER FINAL-STAGED NMOS W/L
(FOR PIXEL-COUNT VGA CLASS)

	USUAL DESIGN (FALL OF SEVERAL ns OR LESS)	EMBODIMENT DESIGN (PRACTICAL VALUE AT FALL OF 40-10ns)
BUFFERS PRESENT ON EACH COLUMN	10/0.6	1/0.6-1/20 (USUAL RATIO 1/10 OR LESS)
BUFFERS PRESENT AT BOTH ENDS OF EACH ROW	6/0.6	1/1-1/20 (USUAL RATIO 1/10 OR LESS)
DRIVING DRN LINES ON THE PIXEL-REGION ENTIRE SURFACE BY ONE BUFFER	5000/0.6	500/0.6-2/20 (USUAL RATIO 1/10 OR LESS)

FIG. 12B

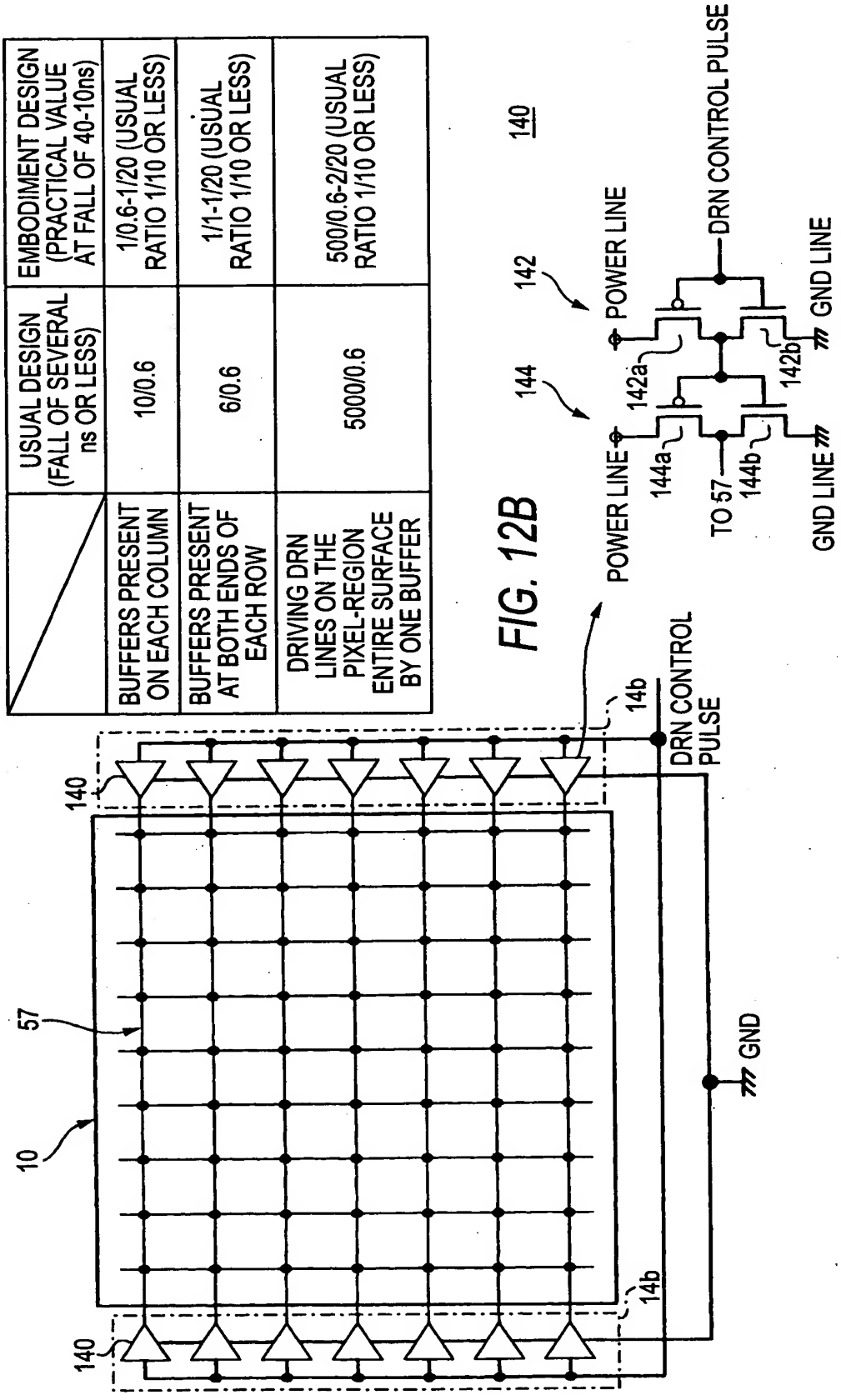

FIG. 12A

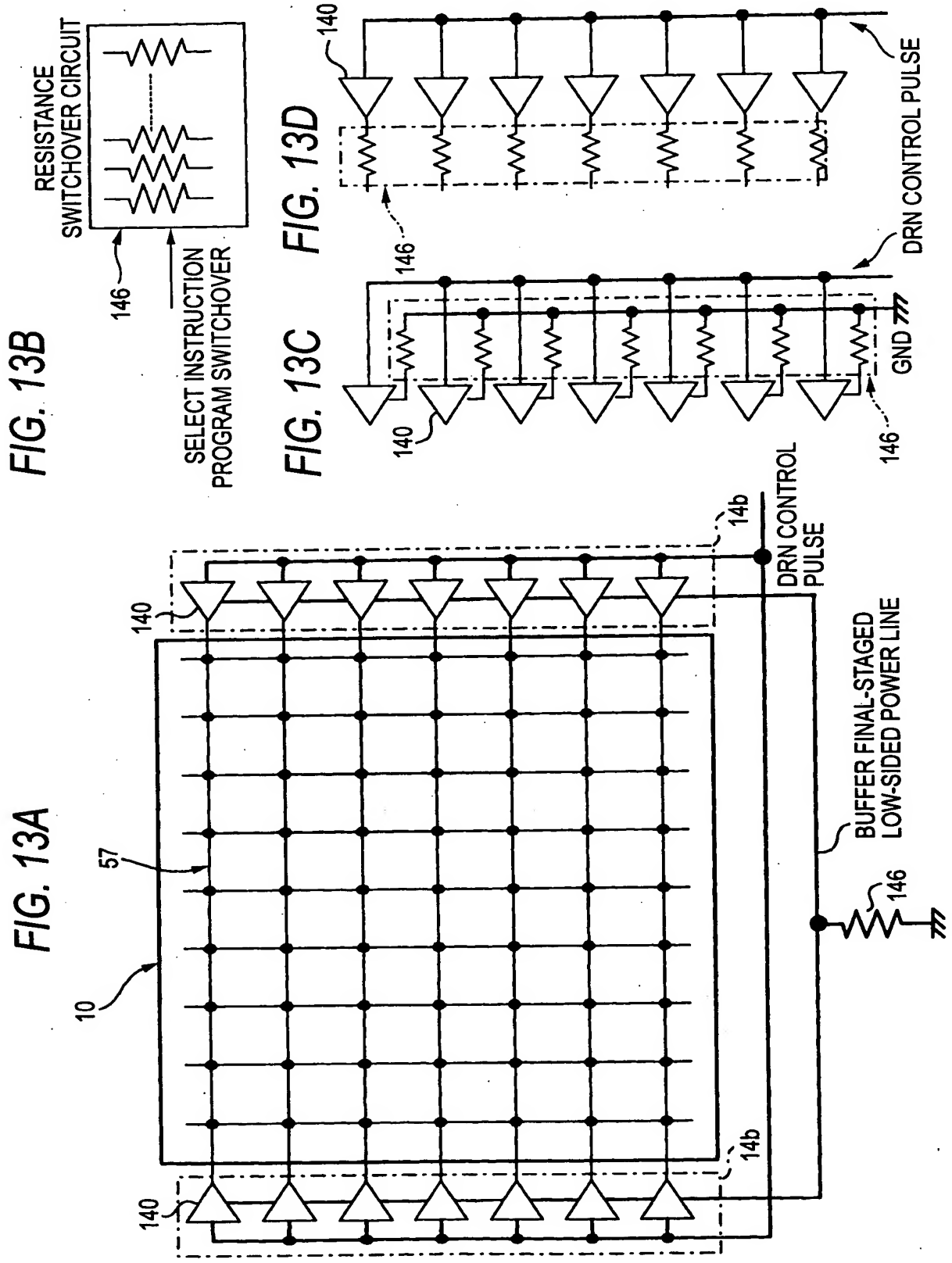
FIG. 13A
10
57
140
140
14b
14b
DRN CONTROL PULSE
BUFFER FINAL-STAGED LOW-SIDED POWER LINE
146
FIG. 13B
RESISTANCE SWITCHOVER CIRCUIT
146
SELECT INSTRUCTION PROGRAM SWITCHOVER
FIG. 13C
140
140
146
GND
FIG. 13D
140
146
DRN CONTROL PULSE

FIG. 14B

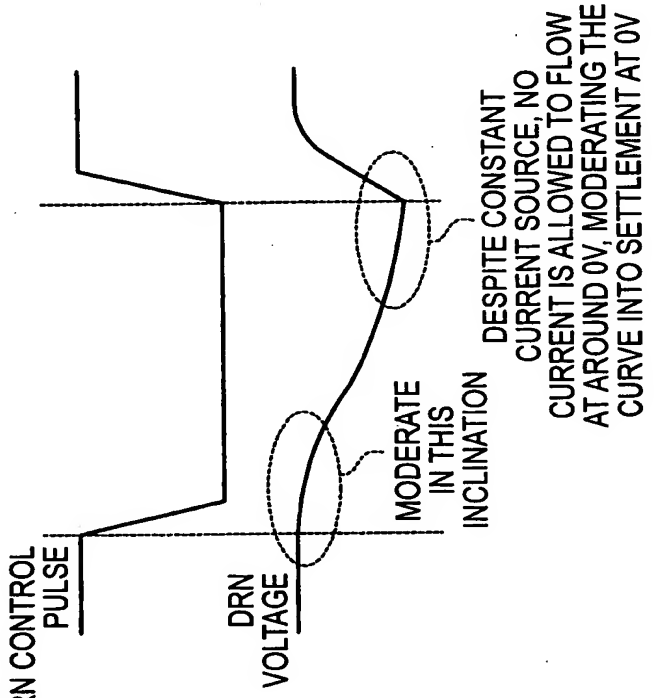

FIG. 14A

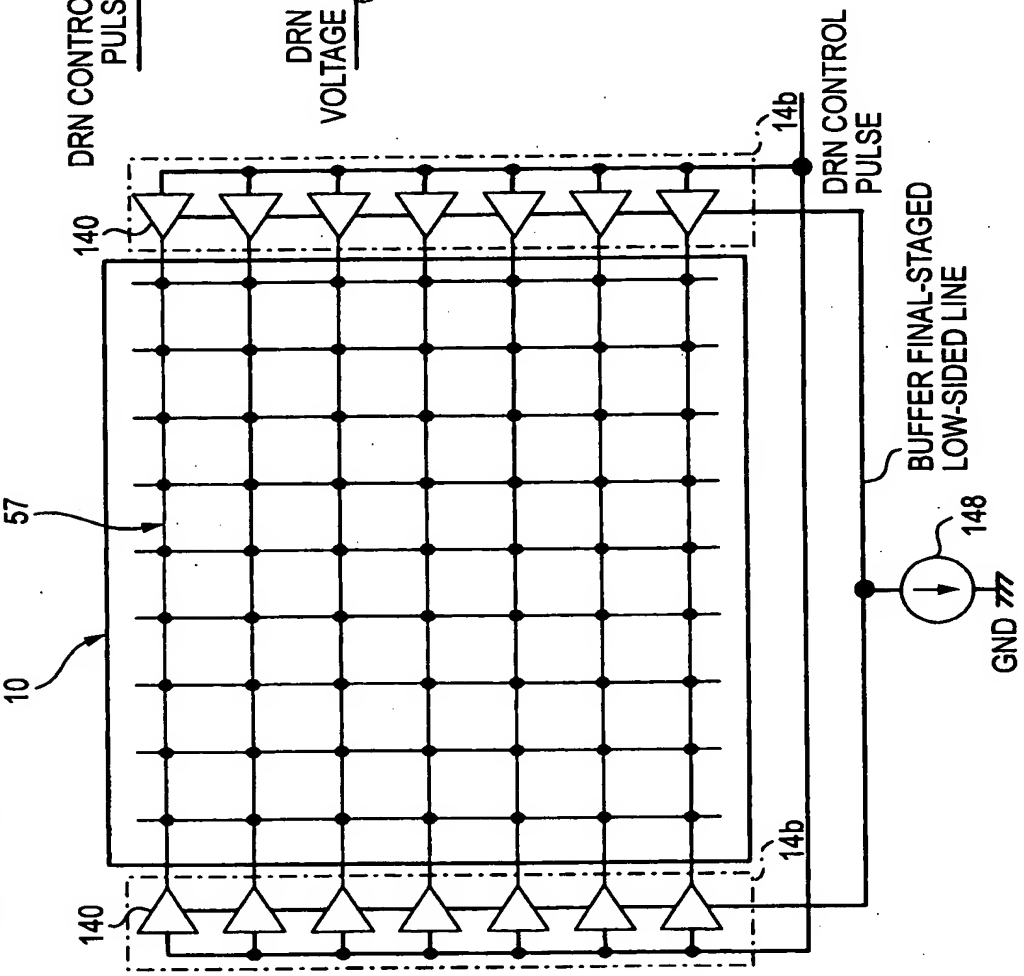

FIG. 15A

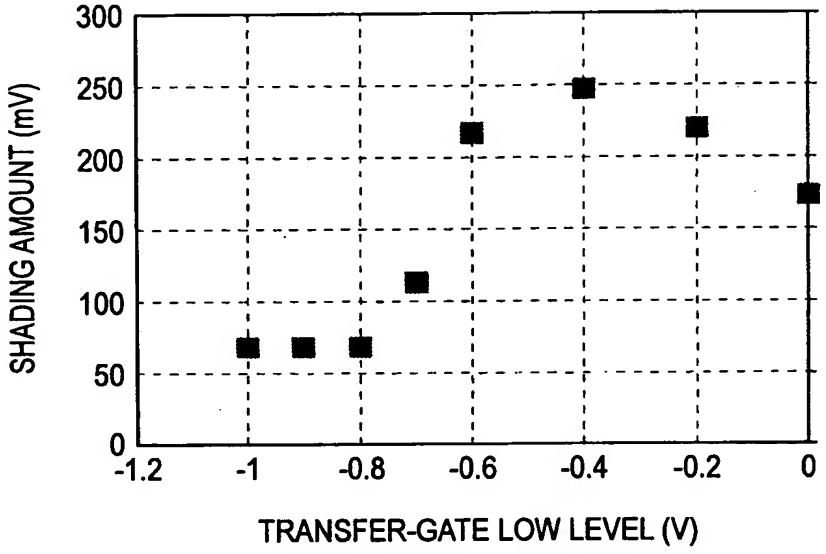

FIG. 15B

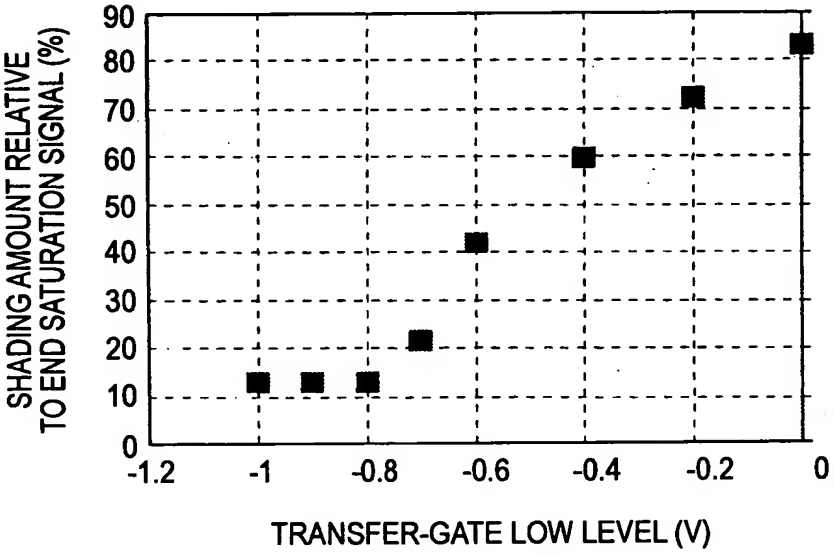

FIG. 16

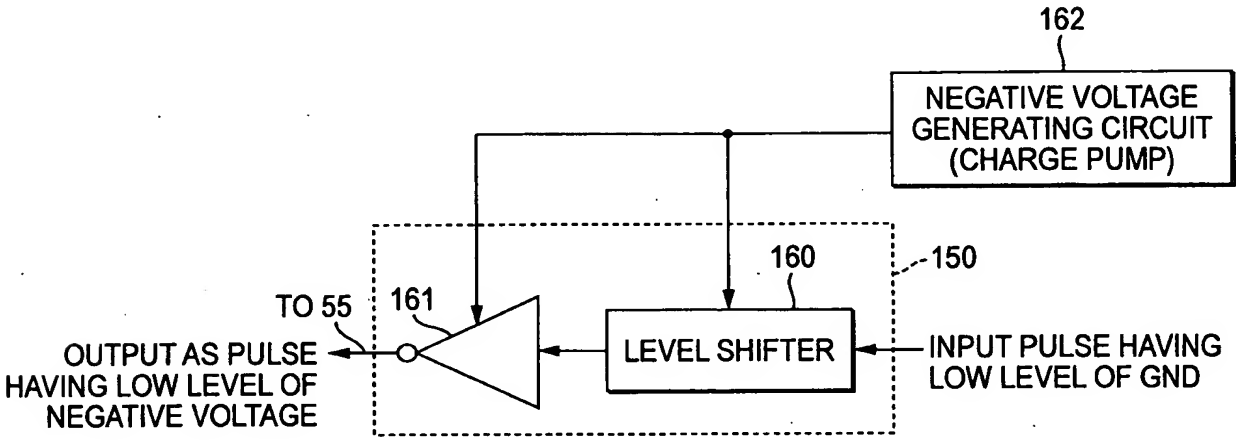
162
NEGATIVE VOLTAGE GENERATING CIRCUIT (CHARGE PUMP)
160
150
TO 55
161
OUTPUT AS PULSE HAVING LOW LEVEL OF NEGATIVE VOLTAGE
LEVEL SHIFTER
INPUT PULSE HAVING LOW LEVEL OF GND

FIG. 17

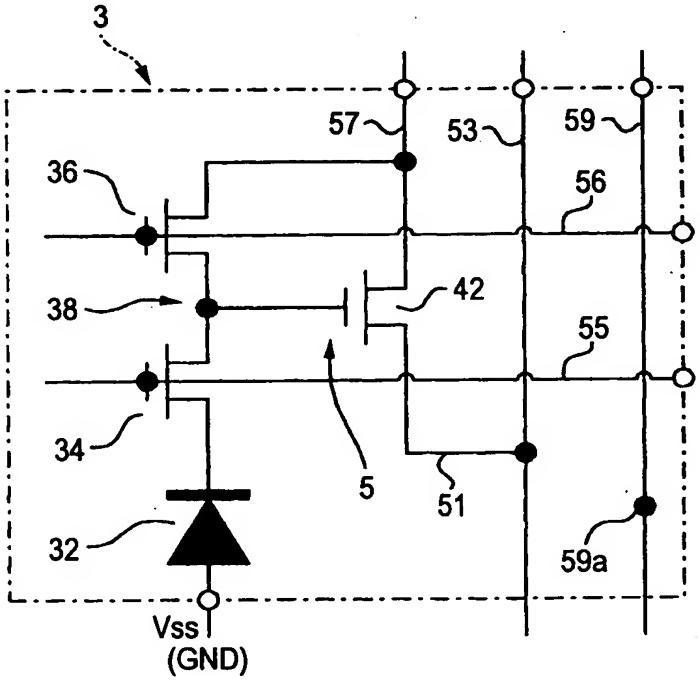
3
57
53
59
36
56
42
38
55
34
5
51
32
59a
Vss
(GND)

FIG. 18A

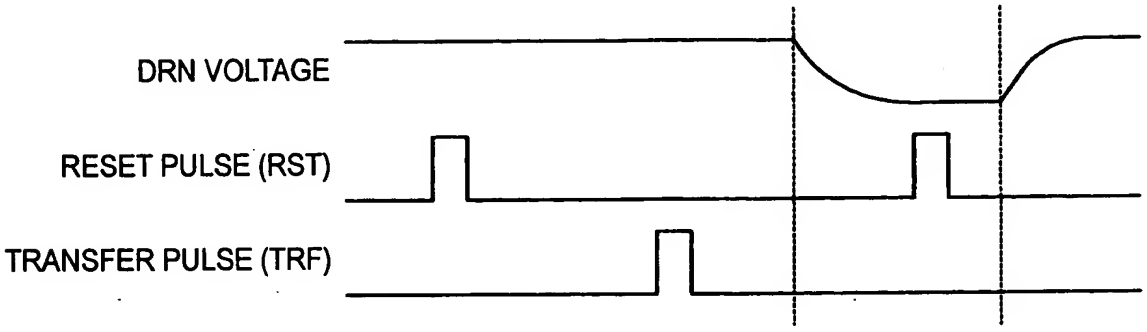

FIG. 18B

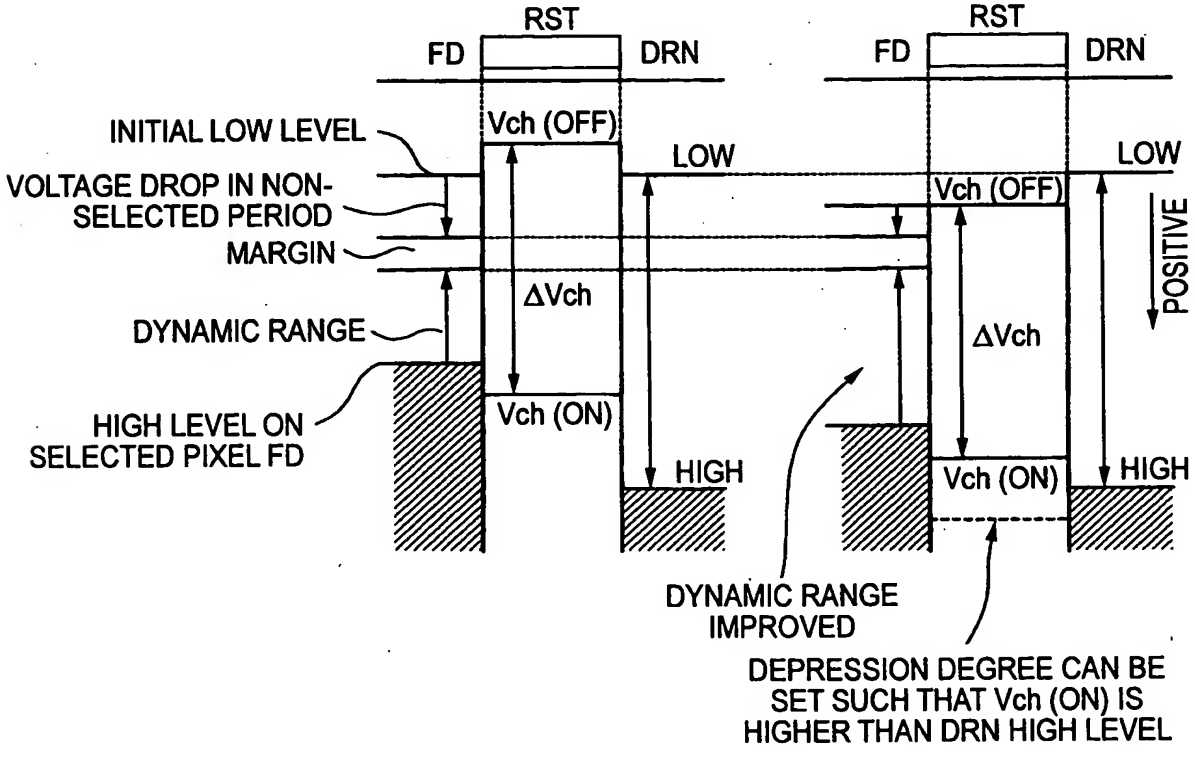

FIG. 18C

FIG. 19A

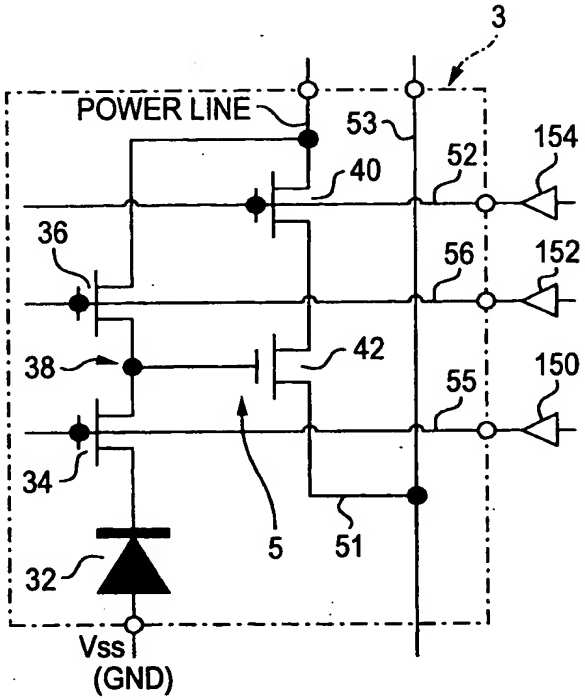

FIG. 19B